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VERIFICATION OF ADVANCED PERIPHERAL BUS IN ADVANCED MICROCONTROLLER BUS ARCHITECTURE USING EDA PLAYGROUND

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Abstract: The Advanced Peripheral Bus (APB) protocol is an important part of the Advanced Microcontroller Bus Architecture (AMBA) family. The APB protocol is a type of testbench communication and design-based testing (DUT) that allows testing. This technique is well-suited for low-cost, low-bandwidth buses with limited electronic devices such as timers and switches. This technique is used to use reusable system-on-chip (SoC) technology to solve problems caused by very large-scale integrated circuits (VLSI). Design and implementation of the APB protocol involves creating cases and developing prototypes using the Verilog Hardware Description Language (HDL) and testing the prototype using the Verilog Test Bench. Open a software like EDA Park. The purpose of the planning study is to develop and implement the AMBA APB protocol using open-source software, focusing on improving the accuracy and efficiency of the design. It also develops a powerful, efficient, and effective system that can be easily integrated into various types of hardware. This study investigates six different experiments involving different change scenarios. Completion of the APB protocol will greatly benefit computer engineering, especially hardware and communication protocols.
Keywords: Advanced Microcontroller Bus Architecture (AMBA), Design-based testing (DUT), The Advanced Peripheral Bus (APB)

Introduction.

1.1 High-end microcontroller bus architecture is widely used in communication systems designed to connect various components in a system-on-chip (SoC) design. The AMBA protocol is used to provide a standard connection between many IP (smart device) standards integrated into the SoC, such as processors, memory controllers and peripheral interfaces. The core of the AMBA protocol is the Advanced Peripheral Bus (APB), a simple, low-power, low-bandwidth interface for connecting low-power devices to the bus. The APB protocol is designed for ease of use and is often used to connect devices such as timers, observer timers, interrupt controllers, and other simple devices. Applications of the APB protocol include understanding the specification process, time requirements, and specific details regarding the implementation of the hardware plan. Compliance with the APB protocol can be a difficult task as it requires creating a design that meets time-based requirements while ensuring the product is of good quality for low energy consumption and high performance. There are many important aspects of the design and implementation of the APB protocol, including the content of the

communication, development of the communication, and verification and testing of the protocol. The design process often involves many iterative steps, including design and implementation, analysis and testing, energy and efficiency. The AMBA protocol suite consists of several protocols, including the High Order Peripheral Bus (APB) protocol. It provides a low-cost and power-efficient interface for connecting low-bandwidth peripherals to the system-on-chip (SoC). AMBA code will support resiliency and reduce the need for silicon infrastructure by supporting the reuse of peripheral devices. The APB protocol is designed for easy connection design and low power consumption, making it a good choice for connecting low-bandwidth peripherals. The combination of switching signals and incremental clocks helps integrate APB peripherals into the design. To enter the programmable control register of an electronic device, the switch must have at least two loops - a setting loop and an access loop. AMBA AHB, AMBA AHB-Lite, AMBA AXI or AMBA AXI4-Lite protocols can be used to create APB interfaces.

APB Block Diagram

1.2 An advanced bus protocol (APB) has been created according to the design, and its features are shown in the block diagram in Fig 1.1

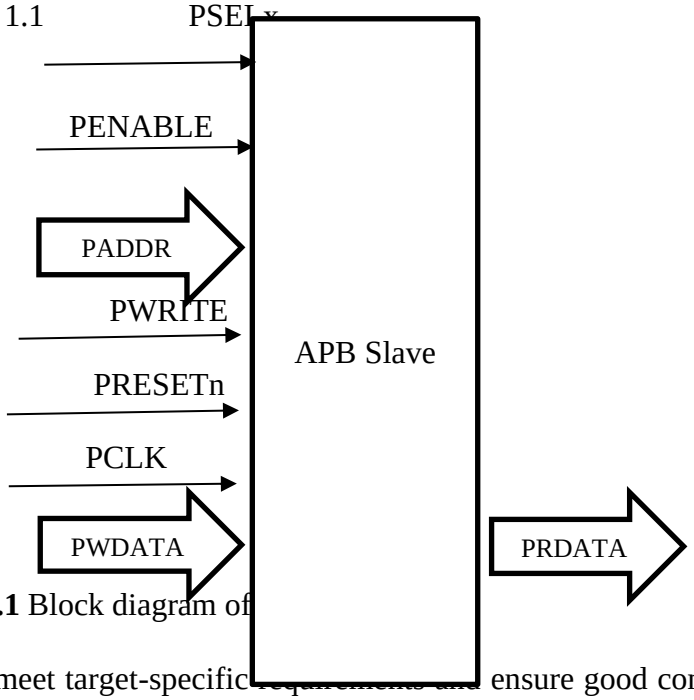

Fig 1.1 Block diagram of

The APB protocol is designed to meet target-specific requirements and ensure good communication between master and slaves. While testing the design in the experiment. A diagram with a detailed diagram showing the main symbols used in the APB protocol.

1.2 APB signals list

The slave part of the APB protocol accepts a variety of input signals, including PCLK, PWRITE, PRESETn, PENABLE, and PSEL, as shown in Figure 1. In return it provides 32 bit PRDATA to the main component. The APB protocol also uses 32-bit PWDATA and PADDR signals as input. Table 1 below provides a detailed description of APB indicators and their functions. APB signals are carefully designed to facilitate efficient communication between main and slave components and enable data transfer during DUT testing.

2. APB PROPOSED WORKING MODEL:

To facilitate read and write operations in the APB, the electronic state machine (FSM) manages its operation in three phases: idle, set, and access. According to previous studies, the process of performing these tasks should not be less than two cycles: the INSTALLATION phase and the ACCESS phase. The first transfer, whether a read or a write, takes three cycles to complete, while

subsequent transfers take only two cycles. The state transition can be seen using the diagram in Figure 2.

2.1 The Idle state

The word "idle" also refers to an earlier state. This means that no action has been taken yet. First of all, all signals including PSEL, PENANBLE and PADDR will not be specified.

The state of SETUP

After spending a single cycle in the SETUP state, the bus normally transitions to the ACCESS state at the next time. When the PENABLE signal is confirmed in the ACCESS state, ACCESS will be activated. When switching from SETUP to ACCESS, writing, saving information, options and addresses must remain constant. According to the ACCESS rule, the PREADY signal sent by the slave determines whether to exit or not.

2.3 Access state

Confirming both the PENABLE and PREADY characters confirms that the transfer has been completed successfully. The values of PADDR, PWRITE, PSEL and PWDATA characters remain constant during access. To complete an operation, simultaneously set the PENABLE and PREADY signals to high (1) in the access state. If further changes are required, the bus will enter the setup phase, and if no further changes are required, the bus will return to its original state (no state).

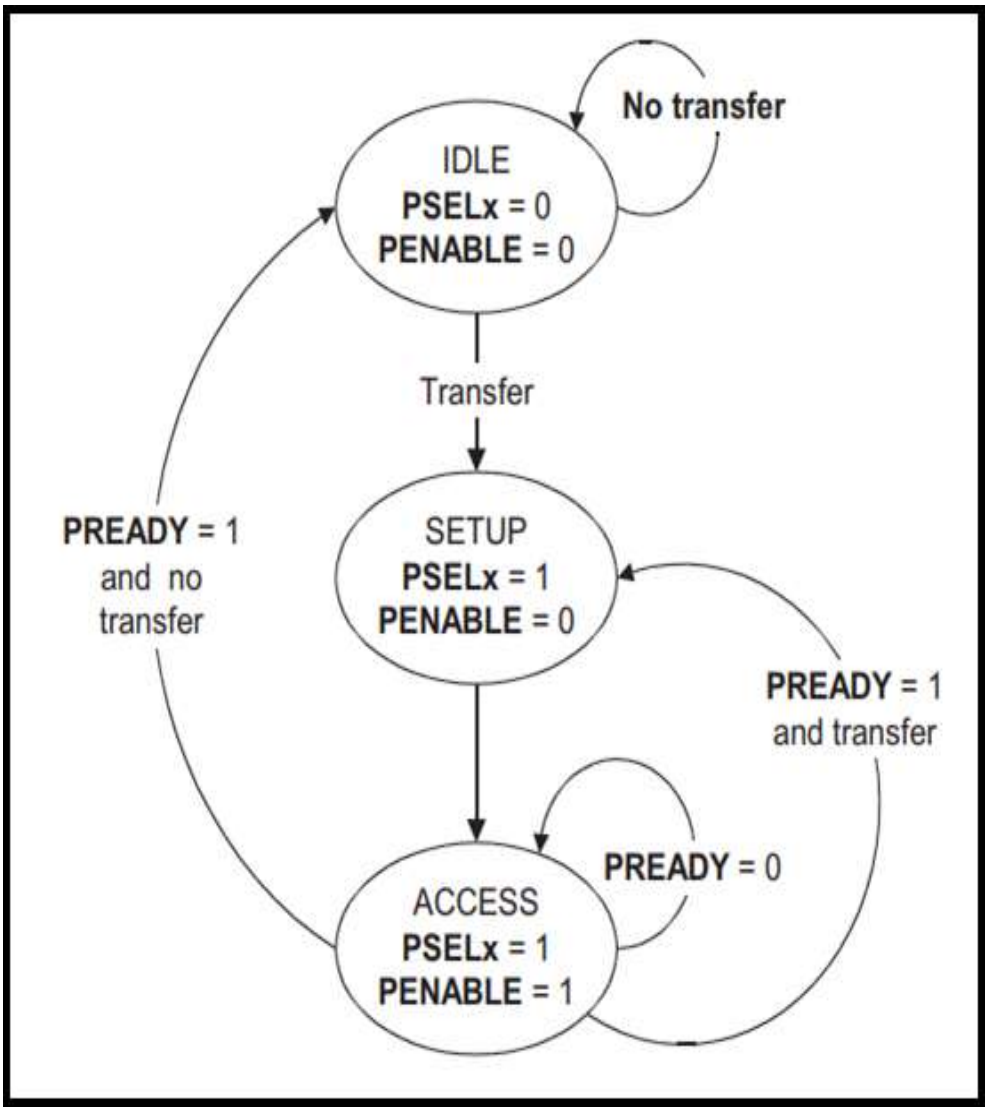

Fig 2.1 APB State diagram

Related work

PROS

1. Peripherals that require less bandwidth such as UART, Keypad, Timer and PIO (Peripheral Input and Output) are connected to the APB.
2. When there is a difference in the arrival time of the clock signal, the time difference will be displayed. Kumar et.al (2017)
3. As technology and SoC designs evolve, the complexity of the design continues to increase and takes on significant workloads. This article explores and examines the various functions and designs in the AMBA, APB, and AXI protocols. Anushka Dwivedi, MD. Anand Jati (2022).
4. A mathematical concept called a finite state machine is sometimes used to design logic or computers. Suan et al. (2019)

5. Design high-level bus systems with the help of Verilog programming language and Verilog Testbench for verification. Future studies will use the best methods to improve the performance of various APB modules. P. Jain and S. Rao (2021).

CONS

1. When devices such as latches and flip-flops store process data, a clock signal is used to synchronize the process. However, changing the time incorrectly can cause 15% to 50% of energy consumption to be wasted. N.Venkateswara Rao (2020).
2.AHB is a brand new AMBA bus designed to meet high performance integrated design needs. D. K. Mishra (2022).

4. APB WRITE AND READ TRANSFER

4.1 Write transfer

During write transfer, PSEL, PWRITE, PADDR and PWDATA signal represent processing elements (also known as SET loop) at clock edge T1. Next. It performs the verification of PENABLE and PENABLE signals at T2 time. This is called the ACCESS loop. If more data needs to be transferred, the PREADY signal changes from high to low at the edge of clock T3 and the PENABLE signal is disabled.

4.2 Write operation using wait

For transaction management, use write operation using wait statement. In this case the PENABLE signal will remain high until the PENABLE signal is also claimed high. The next write will start only when PENABLE and PREADY are declared. According to the wait conditions in Figure 4, the first write will have at least three cycles. Two hours after this condition is completed, typing time returns to normal.

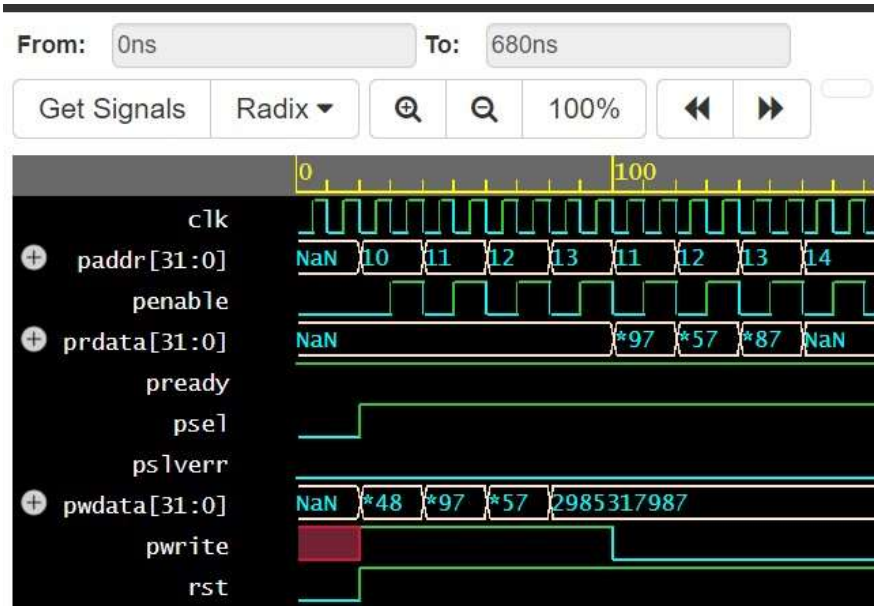

Fig 4.1 Write transfer without wait.

Fig 4.2 Write transfer with wait

4.3 Read transfer without wait

(0) In APB, read changes go through the same steps as write changes. When the PADDR signal is valid, the PRDATA signal is output and updated in the address. During time T0, the start bus is still in IDLE state. At clock edge T1, signals PSEL, PWRITE and PADDR are set high (1) and low
(1) (0) to initiate a readout (setting phase). This setting is the default reading. The PENABLE and PREADY signals are both set high (1) at the following positive clock T3; This indicates that a read on the APB has been completed successfully. As previously mentioned, all readings require at least two hours to complete. If further changes are required, the PENABLE signal decreases and the bus returns to the SETUP state. Figure 5 shows the simultaneous transition of the PREADY signal from high to low in the next reading.

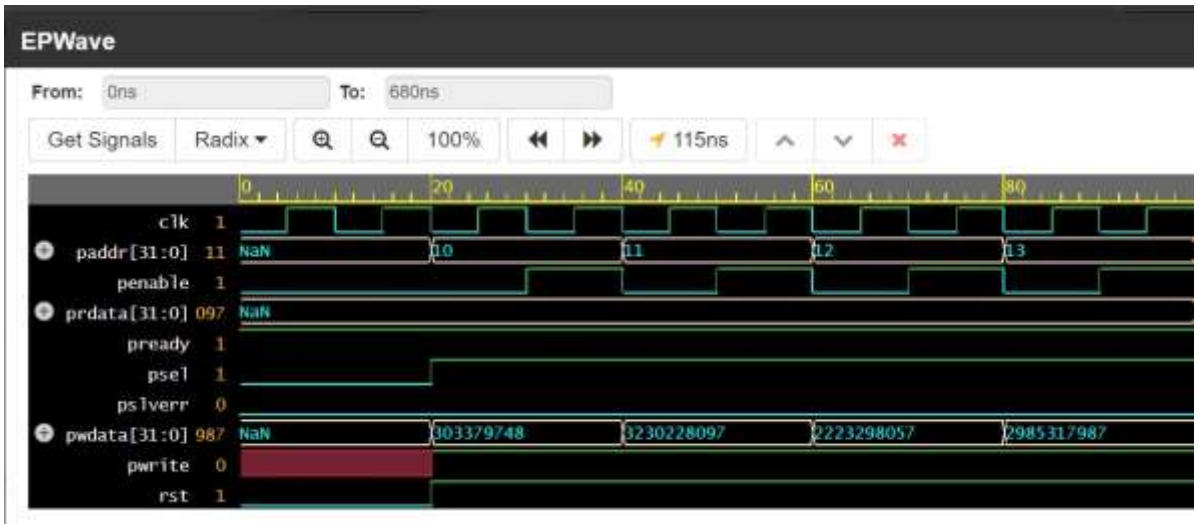

Fig 4.3. Read transfer without wait

4.4 Read transfer with wait

Figure 6 shows a READ transition starting at time T1 using addresses PADDR, PWRITE, and PSEL and recorded on the rising edge of PCLK. Currently, the preparation phase of the transition continues. On the edge of PCLK, after T2, the PENABLE and PEADY signals are displayed. PENABLE signals the beginning of the ACCESS phase, and when confirmed, the slave is informed that it can send PRDATA data in PCLK increment, which will allow the transfer to be completed.

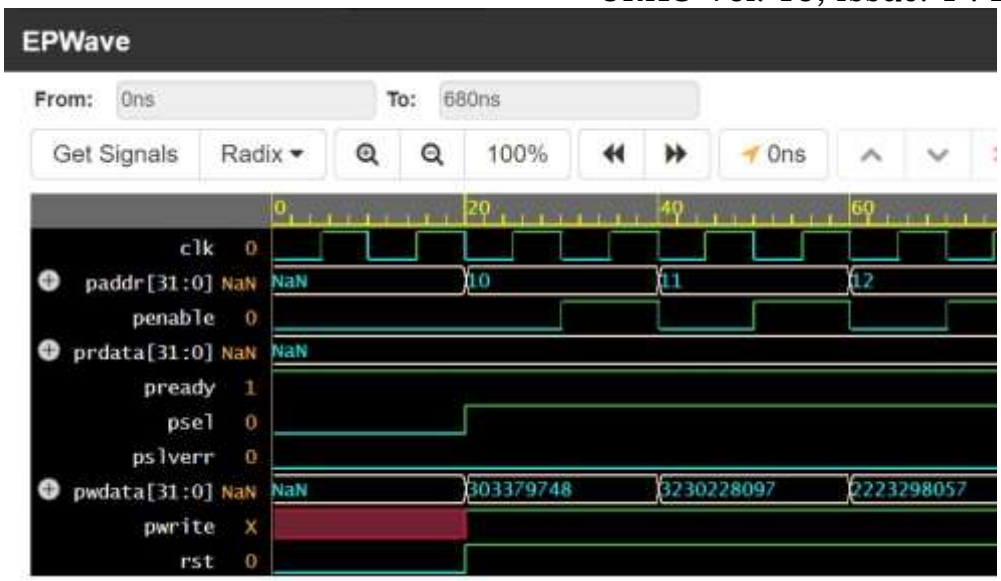

Fig 4.4 Wait statement of Read transfer.

5.Conclusion

In summary, this research paper examines the extension of the AMBA APB protocol, which is widely used in the development of systems-on-chip for communication between peripherals and processors. This article describes the design and operation of the system, including installation time, data transfer process, and various types of business support.

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